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Modified Phase-Shifted PWM Control for Flying Capacitor Multilevel Converters

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***Abstract*—The issue of voltage imbalance remains a challenge for the flying capacitor multilevel converter. The phase-shifted pulsewidth modulation (PS–PWM) method has a certain degree of self-balancing properties. However, the method alone is not sufficient to maintain balanced capacitor voltages in practical applications. The paper proposes a closed-loop modified PS–PWM control method by incorporating a novel balancing algorithm. The algorithm takes advantage of switching redundancies to adjust the switching times of selected switching states and thus maintaining the capacitor voltages balanced without adversely affecting the system's performance. Key techniques of the proposed control method, including selection of switching states, calculation of adjusting times for the selected states, and determination of new switching instants of the modified PS–PWM are described and analyzed. Simulation and experimental results are presented to confirm the feasibility of the proposed method.**

***Index Terms*—Flying capacitor (FC) converter, modified phase-shifted pulsewidth modulation (PS–PWM), multilevel converter, voltage balancing.**

I. Introduction

MULTILEVEL converters synthesize voltage waveforms using a number of semiconductor devices connected in a special arrangement, which are typically rated at a fraction of the dc bus voltage. The unique structure of these multilevel converters makes them suitable for high voltage and high power applications such as flexible alternating current transmission systems (FACTS), high voltage direct current (HVDC), and large electric adjustable speed motor drive (ASMD). These converters are able to generate output voltage waveforms with lower harmonic distortion, lower electromagnetic interference (EMI) and higher efficiencies when compared with the conventional topologies [1]–[3].

There are three types of multilevel converter topologies, namely, the neutral-point-clamped (NPC) converter [4], the flying capacitor (FC) converter [5], and the cascaded converter with separate dc voltage sources (also called H-bridge converter) [6]. The FC converter has attracted a great deal of interest in recent years mainly due to a number of advantageous features. For instance, it seems that the extension of the converter to higher than three levels is possibly easier than the NPC alternative in commercial applications [7], [8]. However, a number of drawbacks need to be further addressed. These include large capacitor banks, additional precharging circuitry, and in particular voltage imbalance amongst FCs.

The balancing of FC voltages is quite important and dictates both the safe and efficient operation of the converter [9]. If voltage imbalance occurs, the quality of the output voltages will deteriorate and blocking voltages imposed on certain devices may increase beyond the rated values. Thus, the safe operation of power devices cannot be guaranteed. Therefore, it is necessary to take into account the balance of FC voltages when designing the control schemes for the FC converters.

Different control strategies taking the capacitor voltage balancing into account have been proposed for FC converters operating in various applications. A direct staircase angle control was introduced in [10]. It is adapted for those applications where the typical pulsewidth modulation (PWM) control does not exist, such as direct torque control (DTC) and sliding mode control or hysteresis control. A carrier-rotation PWM technique was proposed in [11]. However, the above two control methods only deal with the open-loop control. If the small imbalance situation occurs, a compensation algorithm is also needed. A closed-loop control strategy based on an exact linearization and capacitor voltage estimation has been presented in [12]. It remains attractive for dc–dc conversion as it reduces the number of sensors in the converter system. However, its design and implementation becomes complicated and output voltage waveform is affected when applied to dc–ac inverters. The phase-shifted PWM (PS–PWM) method also has a self-balancing property. It has been widely used for the multilevel FC converter since its implementation is straightforward [13]. However, in practical systems, capacitor voltages may diverge from their balanced values due to non-ideal conditions and disturbances, such as unequal capacitance leakage currents, unequal delays in switching, asymmetrical charging/discharging of capacitors and load disturbances. Thus, an external control loop, besides the PS–PWM method is needed to balance the voltage of the capacitors. The integration of an external loop with self-balancing properties is an issue that needs to be further investigated [7].

Some technical papers have presented voltage balancing strategies for FCs based on the PS–PWM method. Specifically, an extra "balance booster" was proposed in [14], which is an RLC filter with a natural frequency equal to the switching frequency to improve the dynamics of rebalancing. It has the advantage of being reliable but the extra filter increases the cost of the overall system and its power losses especially in

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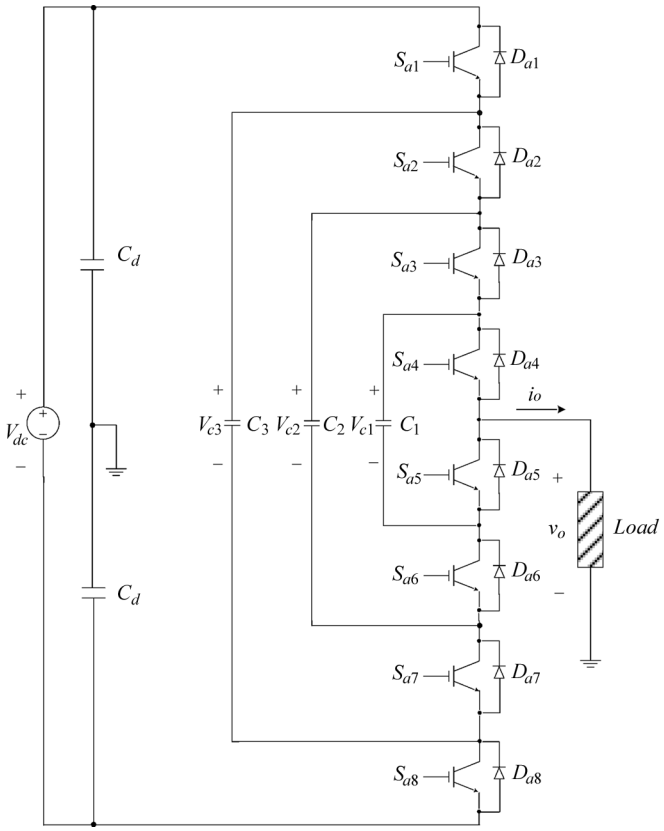

Fig. 1. Phase-leg of a five-level FC multilevel converter.

TABLE I
FIVE-LEVEL FC CONVERTER VOLTAGE LEVELS AND THEIR SWITCHING STATES

v_o	Switching states				Discharging/ charging		
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	C_1	C_2	C_3
$+V_{dc}/2$	1	1	1	1	N	N	N
$+V_{dc}/4$	1	1	1	0	+	N	N
	1	1	0	1	-	+	N
	1	0	1	1	N	-	+
	0	1	1	1	N	N	-
0	1	1	0	0	N	+	N
	1	0	1	0	+	-	+
	0	1	1	0	+	N	-
	1	0	0	1	-	N	+
	0	1	0	1	-	+	-
	0	0	1	1	N	-	N
$-V_{dc}/4$	1	0	0	0	N	N	+
	0	1	0	0	N	+	-
	0	0	1	0	+	-	N
	0	0	0	1	-	N	N
$-V_{dc}/2$	0	0	0	0	N	N	N

1: switch on; 0: switch off;
+: charging mode; −: discharging mode; **N**: no change.
Charging/discharging modes of FCs in this table are obtained assuming $i_o > 0$. These modes are interchanged for $i_o < 0$.

high-voltage applications.Reference [15] proposed a method to either charge or discharge the FCs by switching on switch pairs of positive and negative legs of the multilevel bridge simultaneously for a very short period to maintain capacitor voltages. This method could lead to extremely high short-circuit currents. In [16], a control strategy for five-level multilevel FC converters based on the idea of introducing corrected modulation waveform by adding square-wave type signals was proposed. This control approach can be easily incorporated into the phase-shifted PWM method, but with negative effect on the output waveform. A feedback control scheme was proposed for the voltage stabilization by adding or subtracting duty cycles in proportion to the unbalanced portion [17]. However, it is only suitable for three-level converters with only one FC. For higher-level converters, it is hard to describe the nonlinear relationship between the output current and the capacitor voltages. In addition, there exists interaction among multicapacitors which makes it impossible to control the output current and the capacitor voltages simultaneously by just simply adjusting the respective duty cycles.

The objective of this paper is to present a closed-loop control strategy which consists of the conventional PS–PWM method and a novel voltage balancing control algorithm. The proposed approach is quite different from the above mentioned methods. Specifically, the algorithm utilizes the redundancy of FC converter switching states to change the charge/discharge times of capacitors. In addition, by properly selecting the combinations of the switching states, the method decouples the control of multiple capacitors. Thus, it can control capacitor voltages independently. Moreover, this approach does not introduce any extra harmonic distortion in the output voltage waveform. Even though the proposed control scheme is applied to a five-level FC converter in this paper, it can be extended to higher-level FC converters.

The paper is organized in the following way. Section II describes the basic structure of the five-level FC converter and its operating principle. The conventional PS–PWM method is briefly introduced in Section III. Section IV addresses the proposed voltage balancing control algorithm. Simulation and experimental results with and without the proposed closed-loop control strategy are given in Sections V and VI, respectively, in order to illustrate the validity of the method. Finally, conclusions are summarized in Section VII.

II. FC MULTILEVEL CONVERTER

A phase leg of a five-level FC multilevel converter is shown in Fig. 1. It is vital for the proper functioning of this converter that all FCs, namely, C_1, C_2, and C_3 to be charged to $V_{\rm dc}/4$, $V_{\rm dc}/2$, and $3V_{\rm dc}/4$, respectively. Consequently, the voltage stress across any switch in this circuit equals $V_{\rm dc}/4$. The most attractive feature of the FC converter is that the voltage synthesis in an FC converter has more flexibility than that of the NPC topology. For a given voltage level, there are several switching states that give the same output voltage v_o, but result in different charging or discharging modes for the FCs. This is also known as switching redundancy. Table I lists five-level FC converter's voltage levels and all the charging/discharging modes of each FC for $i_o > 0$. It should be noted that charging/discharging modes of capacitors are interchanged for $i_o < 0$. For the analysis in this paper, the instantaneous load current i_o is assumed to be positive without losing generality. There exist complementary

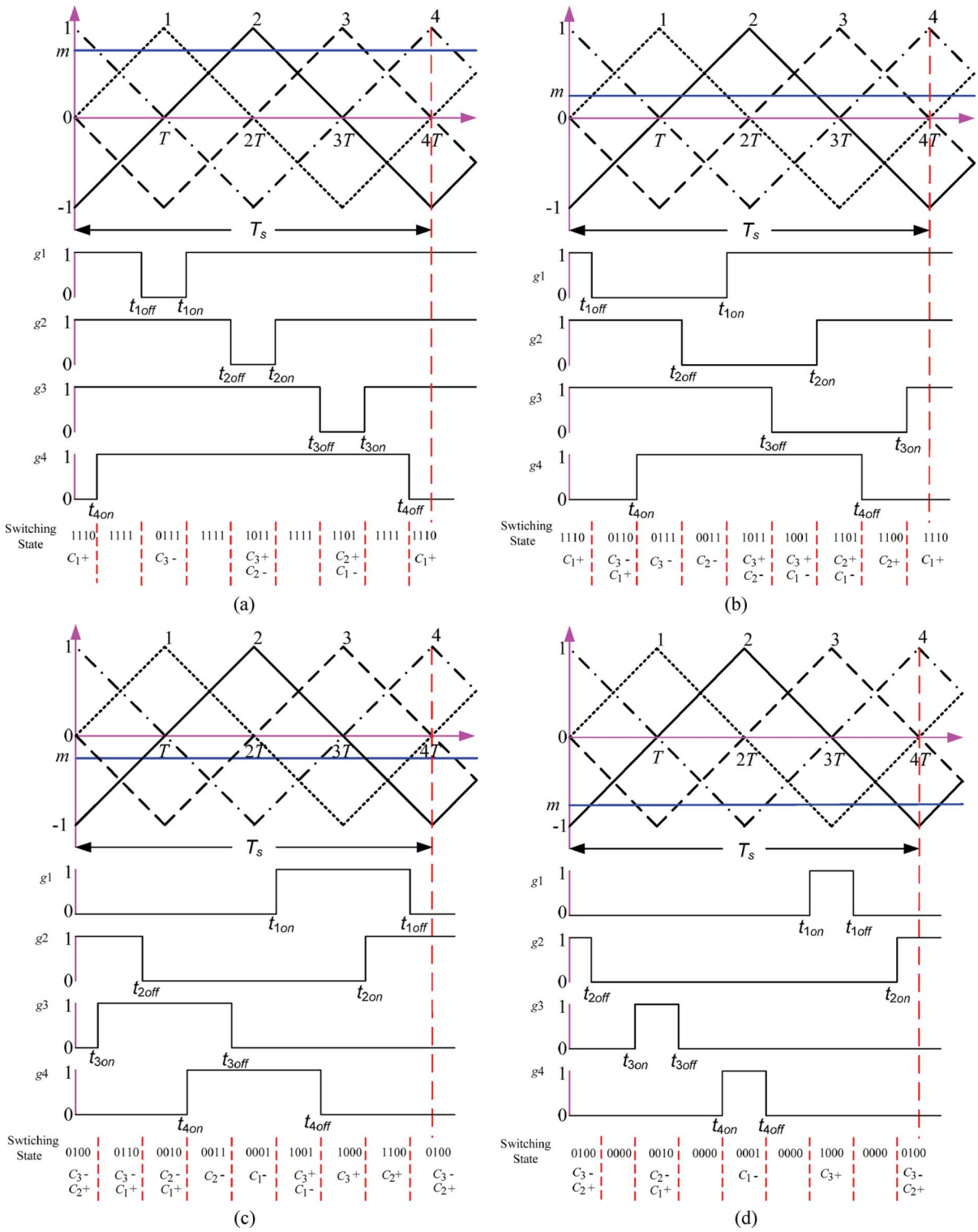

Fig. 2. Control signals for different modulating reference values. (a) 0.5 pu.$< m \leq$ 1.0 pu.; (b) 0 pu.$< m \leq$ 0.5 pu.; (c) -0.5 pu. $< m \leq 0$ pu.; (d) -1 pu. $< m \leq -0.5$ pu.

switch pairs in each phase leg (S_{a1}, S_{a8}), (S_{a2}, S_{a7}), (S_{a3}, S_{a6}) and (S_{a4}, S_{a5}), respectively, but only the upper four switches are given in Table I.

III. Phase-Shifted PWM Method

This concept was first proposed in [18]. For a five-level FC converter, a reference modulation signal is compared with four triangular carrier signals that are phase shifted by 90°. The resulting PWM signals control the corresponding switches.

Fig. 2 illustrates the conventional PS–PWM method applied to a five-level FC converter. It is assumed that the frequency modulation ratio m_f is sufficiently large so that the modulating reference value m can be regarded as a constant in a switching period T_s. There are four regions in terms of the value of m

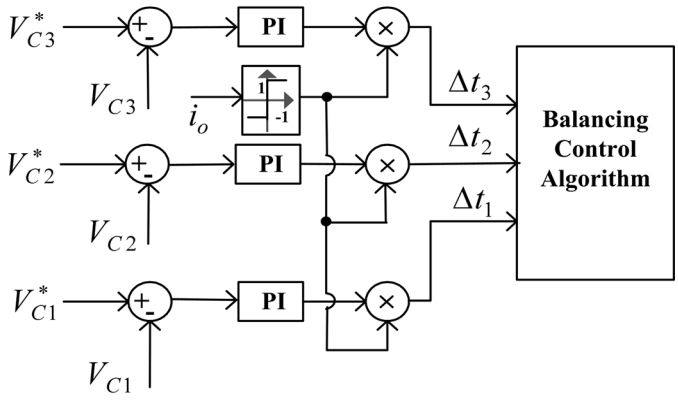

Fig. 3. Building block of the voltage balancing controller.

shown in Fig. 2(a)–(d), respectively. The control switching signals $g1$, $g2$, $g3$, and $g4$ for the main switches of S_{a1} to S_{a4} as well as switching states and associated capacitor charging and discharging modes are also shown in Fig. 2.

PS–PWM can maintain the capacitor voltage to a certain degree by applying equal time duration of the charging and the discharging switching states for each capacitor. Thus, PS–PWM has a self-balancing property. However, voltage imbalance of FCs in practical implementations may still occur due to unequal parameters of the converter caused by different IGBT tolerances, different dv/dt and different value of the FCs, etc. Therefore, a feedback loop is required to eliminate the accumulative error and make the capacitor voltages stabilize at the desired reference values.

IV. Proposed Control Algorithm for Flying Capacitor Voltage Balancing

A. Building Block of the Voltage Balancing Controller

The voltage balancing controller is shown in Fig. 3. It consists of proportional integral (PI) controllers and a balancing control algorithm. This novel algorithm is introduced in this section. Here, the reference voltages V_{C1}^*, V_{C2}^*, and V_{C3}^* for the three FCs in the five-level FC converter are $V_{\rm dc}/4$, $V_{\rm dc}/2$, and $3V_{\rm dc}/4$, respectively. The actual average values of V_{C1}, V_{C2}, and V_{C3} measured by sensors are compared with their reference values and then the errors are fed into the PI controllers. The outputs of the PI controllers are multiplied with the sign of the output current i_o and finally generate the adjusting time Δt_1, Δt_2, and Δt_3 for the FCs C_1, C_2, and C_3, respectively. The load current direction must be considered since it determines the capacitor charging or discharging mode for the same switching state.

The implementation procedure of the balancing control algorithm can be summarized as follows.

Step 1: Selecting the related switching states to be adjusted for compensating the voltage variation for every FC in terms of different regions.

Step 2: Calculating the adjusting time Δt for every selected switching state taking Δt_3, Δt_2, and Δt_1 into account.

Step 3: Adjusting the time duration of every selected switching state and determining switching instants.

B. Implementation of the Novel Voltage Balancing Control Algorithm

Step 1: As illustrated in Fig. 2, there are four regions in terms of m. For every region, different switching states are selected to compensate the capacitor voltage variations. Taking the region 0.5 pu. $< m \leq$ 1.0 pu. as an example, five switching states are available according to PS–PWM, namely 1110, 1111, 0111, 1011, and 1101, as shown in Fig. 2(a). Assuming V_{C1} is lower than its reference value, it is required to increase V_{C1} while not affecting V_{C2} and V_{C3}. One possible way is just to increase the time duration of 1110 so as to increase the charging time of C_1 and thus to increase V_{C1}. However, increasing the 1110 duration decreases the 1111 duration, and the duty cycle is changed, thus the output voltage is affected through this simple adjustment. To ensure the output voltage is not affected, all of the switching instants in a switching cycle need to be considered to force V_{C1} to return back to its reference value without affecting V_{C2}, V_{C3} and the output voltage as well. It can be seen from the Table I that the switching state 1101 discharges C_1 and charges C_2 in this region. We can reduce the time duration of this state by $\Delta t_1/4$ so that the C_1 discharge time is reduced by $\Delta t_1/4$ which increases V_{C1}. However, such an adjustment affects V_{C2} since it shortens the charging time of C_2. To compensate that, the 1011 switching state can be shortened by $\Delta t_1/4$. The adjustment of the state 1011 in turn decreases V_{C3}. Then, we can compensate the variation of V_{C3} by shortening the 0111 switching state by $\Delta t_1/4$. Therefore, by shortening the switching states 1101, 1011, and 0111 by $\Delta t_1/4$, respectively, V_{C1} is increased without affecting V_{C2} and V_{C3} values. Finally, in order to keep the duty cycle in a switching period unchanged, the duration of the switching state 1110 must be increased by $3\Delta t_1/4$, which further increases the charging time of C_1 and V_{C1}. The adjusted waveforms are shown in Fig. 4.

Similarly, V_{C2} and V_{C3} can be adjusted through selecting the appropriate switching states. When the modulating reference value is between 0.5 and 1.0 pu., their adjustment procedure can be explained as follows.

If V_{C1} is lower than its reference value, then:

- reduce the time duration of the state 1101 by $\Delta t_1/4$ (i.e., C_1 discharging time decreases, C_2 charging time also decreases);
- reduce the time duration of the state 1011 by $\Delta t_1/4$ (i.e., C_2 discharging time decreases, C_3 charging time also decreases);
- reduce the time duration of the state 0111 by $\Delta t_1/4$ (i.e., C_3 discharging time decreases);
- increase the time duration of the state 1110 by $3\Delta t_1/4$ (i.e., C_1 charging time increases).

If V_{C2} is lower than its reference value, then:

- increase the time duration of the state 1101 by $\Delta t_2/2$ (i.e., C_2 charging time increases, C_1 discharging time also increases);
- increase the time duration of the state 1110 by $\Delta t_2/2$ (i.e., C_1 charging time increases);
- reduce the time duration of the state 1011 by $\Delta t_2/2$ (i.e., C_2 discharging time decreases, C_3 charging time also decreases);
- reduce the time duration of the state 0111 by $\Delta t_2/2$ (i.e., C_3 discharging time decreases).

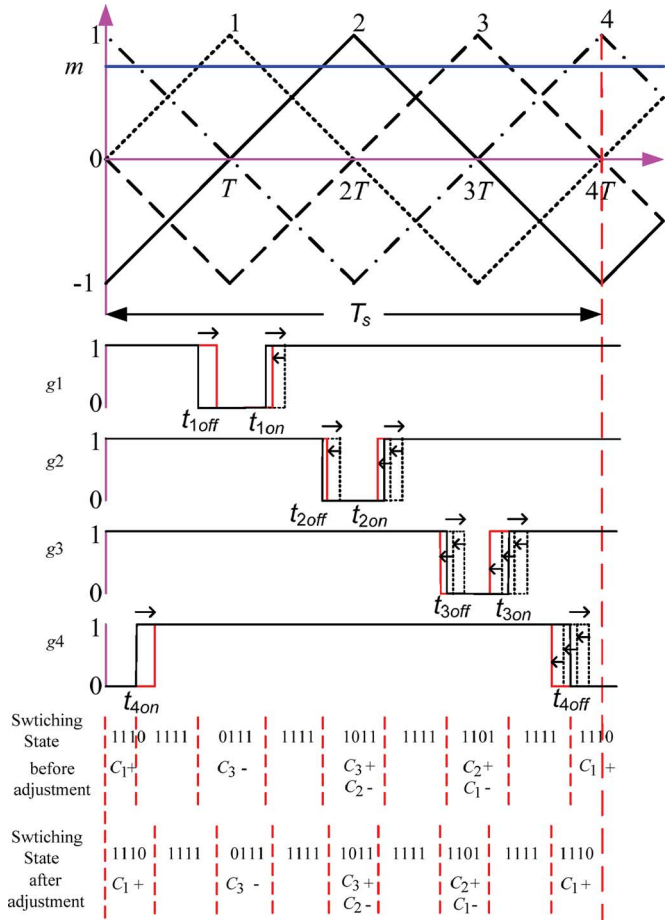

Fig. 4. Expanded view of selected switching waveforms after adjustment.

If V_{C3} is lower than its reference value, then:

- increase the time duration of the state 1011 by $\Delta t_3/4$ (i.e., C_3 charging time increases, C_2 discharging time also increases);
- increase the time duration of the state 1101 by $\Delta t_3/4$ (i.e., C_2 charging time increases, C_1 discharging time also increases);
- increase state 1110 length by $\Delta t_3/4$ (i.e., C_1 charging time increases);
- reduce state 0111 length by $3\Delta t_3/4$ (i.e., C_3 discharging time decreases).

The adjusting times of selected switching states for all four regions are summarized in Table II. The overall adjusting times during a switching period for any region is zero in order to avoid changing the output voltage and affecting the overall system characteristics. It should be mentioned that Table II is valid for any capacitor voltage and load current though it is assumed in the analysis that capacitor voltages are smaller than the reference values and the load current is positive, because Δt_1, Δt_2, and Δt_3 contain the information on the variation of the capacitor voltages and the sign of the load current through the controller in Fig. 3.

Step 2: The total adjusting time Δt for every selected switching state can be obtained by summing the adjusting times for all capacitors as listed in Table III. According to PS–PWM, the width of each state, i.e., the time duration t is a function of

TABLE II
ADJUSTMENT OF SELECTED SWITCHING STATES FOR INDIVIDUAL CAPACITORS

m		Switching states/Adjusting time					
(pu.)		**1101**	**1011**	**0111**	**1110**	**1100**	**0011**
0.5	C_1	$-\Delta t_1/4$	$-\Delta t_1/4$	$-\Delta t_1/4$	$3\Delta t_1/4$		
to	C_2	$\Delta t_2/2$	$-\Delta t_2/2$	$-\Delta t_2/2$	$\Delta t_2/2$		
1.0	C_3	$\Delta t_3/4$	$\Delta t_3/4$	$-3\Delta t_3/4$	$\Delta t_3/4$		
0.0	C_1	$-\Delta t_1/4$	$-\Delta t_1/4$	$-\Delta t_1/4$	$3\Delta t_1/4$		
to	C_2					$\Delta t_2/2$	$-\Delta t_2/2$
0.5	C_3	$\Delta t_3/4$	$\Delta t_3/4$	$-3\Delta t_3/4$	$\Delta t_3/4$		
		0010	**0100**	**1000**	**0001**	**0011**	**1100**
-0.5	C_1	$\Delta t_1/4$	$\Delta t_1/4$	$\Delta t_1/4$	$-3\Delta t_1/4$		
to	C_2					$-\Delta t_2/2$	$\Delta t_2/2$
0.0	C_3	$-\Delta t_3/4$	$-\Delta t_3/4$	$3\Delta t_3/4$	$-\Delta t_3/4$		
-1.0	C_1	$\Delta t_1/4$	$\Delta t_1/4$	$\Delta t_1/4$	$-3\Delta t_1/4$		
to	C_2	$-\Delta t_2/2$	$\Delta t_2/2$	$\Delta t_2/2$	$-\Delta t_2/2$		
-0.5	C_3	$-\Delta t_3/4$	$-\Delta t_3/4$	$3\Delta t_3/4$	$-\Delta t_3/4$		

m, which is also listed in Table III. The time duration of a state after adjustment $t + \Delta t$ should not be less than zero, otherwise the state would not exist any longer and would result in errors of PWM switching. $t + \Delta t$ of a state should also not be larger than a maximum value which could result in a negative value of $t + \Delta t$ of another state, but if $t + \Delta t \geq 0$ for all states, $t + \Delta t$ has been limited to be less than the maximum value automatically because the overall adjusting time is zero. Thus, only the following condition should be met for all states:

$$\Delta t \geq -t. \tag{1}$$

If $\Delta t < -t$, then it must be normalized to the width t

$$\Delta t_{\text{new}} = -t = \Delta t \cdot k \tag{2}$$

where $k = -t/\Delta t$. Correspondingly, all other adjusting times also multiply the same coefficient k to guarantee the overall adjusting time in any region being zero.

Step 3: There can be various methods to adjust the time duration of selected switching states and determine switching instants. The method used in this paper is to adjust states from left to right and to shift only switching instants on the right of a selected state. The region of 0.5 pu. $< m \leq$ 1.0 pu. is once again used as an example to illustrate the method of adjusting time duration of every selected state. For any Δt_1, Δt_2, and Δt_3, the adjusting time Δt for all four states in this region can be calculated by using formulas in Table III. Assuming $\Delta t_1 > 0$ and $\Delta t_2 = \Delta t_3 = 0$ to adjust V_{C1} only, the adjusting time Δt is $-\Delta t_1/4$ for the state 1101, $-\Delta t_1/4$ for 1011, $-\Delta t_1/4$ for 0111, and $3\Delta t_1/4$ for 1110, respectively. The switching states before adjustment are obtained using the conventional PS–PWM method as shown in Fig. 4. For the state 1110, since it is distributed at both ends of each cycle, the time duration at the left end is increased by half of $3\Delta t_1/4$, i.e., t_{4on} is shifted right by $3\Delta t_1/8$. At the same time, all other switching instants on the right of t_{4on} (including t_{1off}, t_{1on}, t_{2off}, t_{2on}, t_{3off},

TABLE III
ADJUSTING TIME OF SELECTED SWITCHING STATES AND THEIR TIME DURATION

m (pu.)	Switching states	Adjusting time Δt	Width t
0.5 to 1.0	1101	$-\Delta t_1/4+\Delta t_2/2+\Delta t_3/4$	$(2-2m)T$
	1011	$-\Delta t_1/4-\Delta t_2/2+\Delta t_3/4$	$(2-2m)T$
	0111	$-\Delta t_1/4-\Delta t_2/2-3\Delta t_3/4$	$(2-2m)T$
	1110	$3\Delta t_1/4+\Delta t_2/2+\Delta t_3/4$	$(2-2m)T$
0.0 to 0.5	1101	$-\Delta t_1/4+\Delta t_3/4$	$2mT$
	1011	$-\Delta t_1/4+\Delta t_3/4$	$2mT$
	0111	$-\Delta t_1/4-3\Delta t_3/4$	$2mT$
	1110	$3\Delta t_1/4+\Delta t_3/4$	$2mT$
	0011	$-\Delta t_2/2$	$(1-2m)T$
	1100	$\Delta t_2/2$	$(1-2m)T$
-0.5 to 0.0	0010	$\Delta t_1/4-\Delta t_3/4$	$-2mT$
	0100	$\Delta t_1/4-\Delta t_3/4$	$-2mT$
	1000	$\Delta t_1/4+3\Delta t_3/4$	$-2mT$
	0001	$-3\Delta t_1/4-\Delta t_3/4$	$-2mT$
	0011	$-\Delta t_2/2$	$(1+2m)T$
	1100	$\Delta t_2/2$	$(1+2m)T$
-1.0 to -0.5	0010	$\Delta t_1/4-\Delta t_2/2-\Delta t_3/4$	$(2+2m)T$
	0100	$\Delta t_1/4+\Delta t_2/2-\Delta t_3/4$	$(2+2m)T$
	1000	$\Delta t_1/4+\Delta t_2/2+3\Delta t_3/4$	$(2+2m)T$
	0001	$-3\Delta t_1/4-\Delta t_2/2-\Delta t_3/4$	$(2+2m)T$

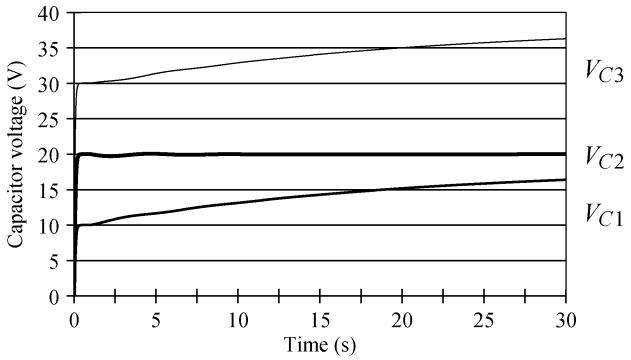

Fig. 5. FC voltages with the conventional PS–PWM method.

t_{3on}, and t_{4off}) are shifted right by $3\Delta t_1/8$. For the state 0111, only its right switching instant, i.e. t_{1on} is shifted left by $\Delta t_1/4$. At the same time, all other switching instants on the right of t_{1on} (including t_{2off}, t_{2on}, t_{3off}, t_{3on}, and t_{4off}) are shifted left by $\Delta t_1/4$. For the state 1011, only its right switching instant, i.e. t_{2on} is shifted left by $\Delta t_1/4$. At the same time, all other switching instants on the right of t_{2on} (including t_{3off}, t_{3on}, and t_{4off}) are shifted left by $\Delta t_1/4$. For the state 1101, t_{3on} is shifted left by $\Delta t_1/4$. At the same time, t_{4off} is shifted left by $\Delta t_1/4$. After these adjustments, it can be known that the time duration of 1110 at the right end has actually increased by $3\Delta t_1/8$, which means the total time duration for 1110 increases by $3\Delta t_1/4$ as required. Therefore, new switching instants for all states after adjustment can be obtained and shown in Fig. 4.

V. SIMULATION RESULTS

To verify the performance of the voltage balancing control algorithm, simulations are carried out on a single-phase five-level FC converter. Parameters of the converter system are: $V_{\rm dc} = 40$ V, $V_{C3}^* = 30$ V, $V_{C2}^* = 20$ V, $V_{C1}^* = 10$ V, $f_o = 50$ Hz, $f_s = 1600$ Hz, $C_1 = C_2 = C_3 = 1500$ μF; Load: $R = 15$ Ω, $L = 20$ mH; PI controller: $K_P = 10^{-6}$, $K_I = 2 \times 10^{-7}$. Here, f_o is the fundamental frequency, or modulating frequency, f_s is the carrier frequency or the switching frequency.

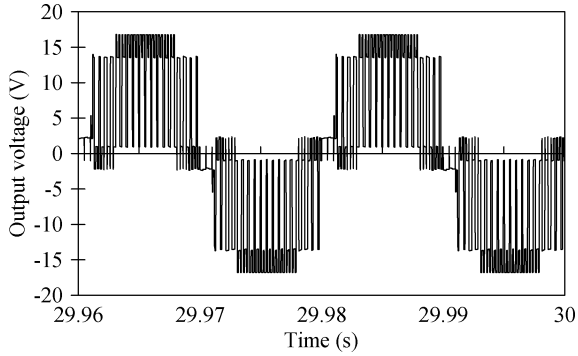

Fig. 6. Phase output voltage v_o with the conventional PS–PWM method (THD=15.9%).

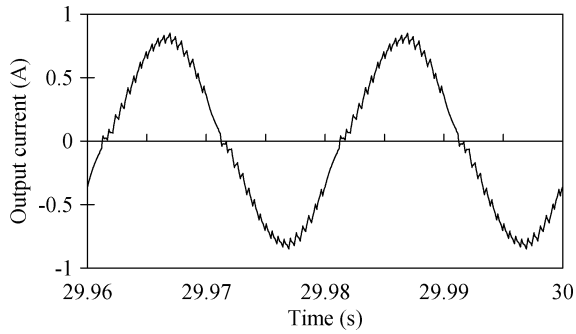

Fig. 7. Phase output current i_o with the conventional PS–PWM method (THD=6.7%).

In simulations, from 0 to 1 s, voltages of FCs V_{C1}, V_{C2}, and V_{C3} are charged to their balance points, i.e., 10, 20, and 30 V respectively through an external charging circuit. After 1 s, the external charging circuit is disconnected and the conventional PS–PWM method starts to work and generates a 50-Hz sinusoidal output voltage v_o. The amplitude modulation ratio of v_o is $m_a = 0.8$. Since there is no feedback control, capacitor voltages have deviated from their balance points as shown in Fig. 5. Especially V_{C1} and V_{C3} have increased to 17 V and 37 V. The output voltage v_o and output current i_o have deteriorated, as shown in Figs. 6 and 7. After 30 s, the modified PS–PWM method starts to operate, and capacitor voltages are controlled back to their balance points, as shown in Fig. 8. Waveforms of v_o and i_o shown in Figs. 9 and 10 are thus significantly improved. The total harmonic distortion (THD) of v_o decreases from 15.9% to 13.1% and the THD of i_o decreases from 6.7% to 5.3%.

VI. EXPERIMENTAL RESULTS

Experimental tests are conducted to replicate the tests performed in simulations. A low-power single-phase five-level FC converter prototype is built. The TMS320LF2407 digital signal processor (DSP) EVM board from Texas Instruments (TI) is

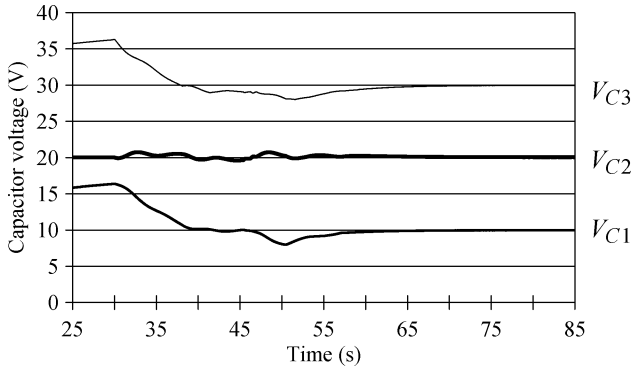

Fig. 8. FC voltages with the modified PS–PWM method.

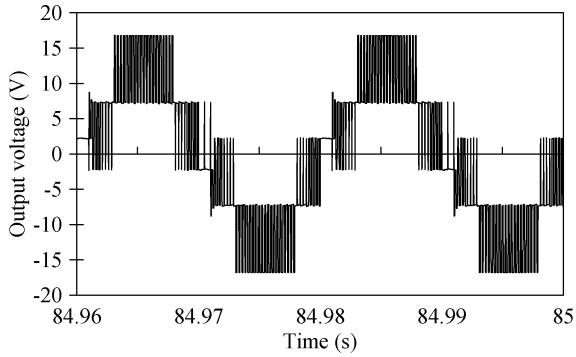

Fig. 9. Phase output voltage v_o with the modified PS–PWM method (THD=13.1%).

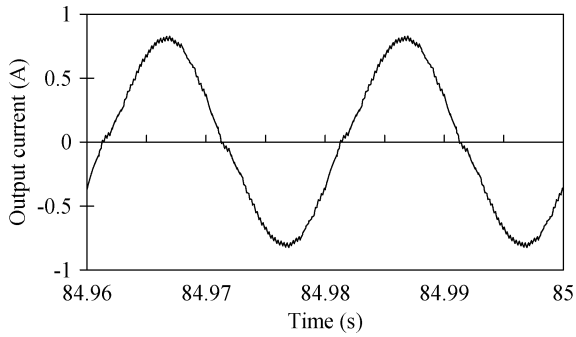

Fig. 10. Phase output current i_o with the modified PS–PWM method (THD=5.3%).

used in order to provide the control solution. The parameters of the converter prototype, load conditions and controllers are the same as those used in simulations.

Fig. 11 shows the voltage waveforms of the three FCs before and after the modified PS–PWM control method takes action. In the captured oscilloscope window, the conventional PS–PWM method operates until 20 s, and the voltage imbalance can be observed. The capacitor voltages have deviated to 16, 20.5, and 36 V, respectively from their balance points. From 20 s the modified PS–PWM method starts to operate, and the capacitor voltages are controlled back to balance points. Figs. 12 and 13 give the waveforms of the output voltage and current with the PS–PWM method and with the modified PS–PWM method, respectively, for a comparison. The waveform quality has been improved with the modified PS–PWM method.

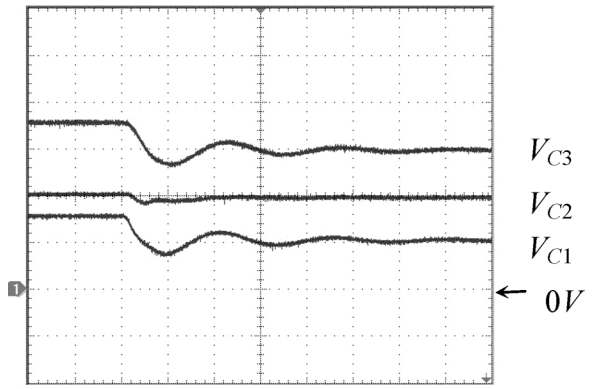

Fig. 11. FC voltages with the conventional PS–PWM method before 20 s and with the modified PS–PWM method after 20 s. Scales of oscilloscope: 10 V/div and 10 s/div.

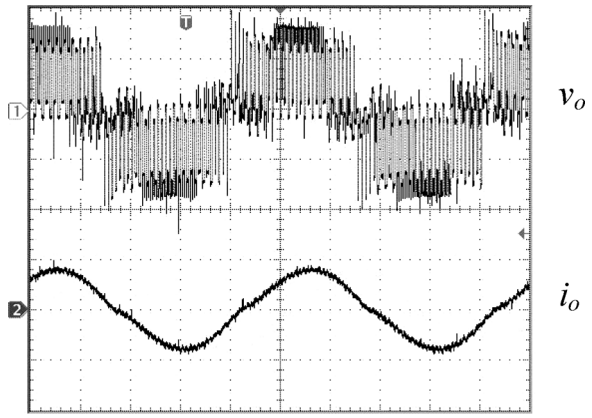

Fig. 12. Output voltage and current with the conventional PS–PWM method. Ch1: v_o (10 V/div); Ch2: i_o (1 A/div); time (4 ms/div).

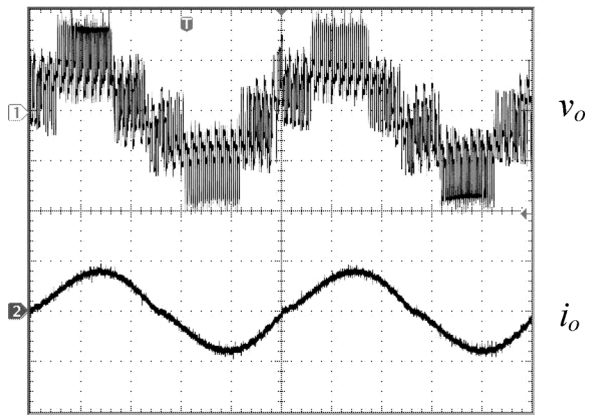

Fig. 13. Output voltage and current with the modified PS–PWM method. Ch1: v_o (10 V/div); Ch2: i_o (1 A/div); time (4 ms/div).

VII. Conclusion

The imbalance problem exists in multilevel FC converters using the phase-shifted PWM method. A modified PS–SPWM control method for a five-level FC inverter has been presented in the paper. This closed-loop method consists of PI controllers and a voltage balancing algorithm. The algorithm utilizes the redundancy of switching states of FC converters, adjusts the time duration of selected switching states, and modifies switching

instants of PS–PWM so as to compensate for the deviation of the capacitor voltages. The proposed method can maintain balanced voltages of FCs, which contributes to both the quality of the output voltages and safe operation of the converter. In summary, the method has the following features.

- The overall adjusting time is zero in each switching period in order to keep the duty cycle unchanged. Therefore, the output voltage performance is not affected by such an adjustment.
- Each capacitor voltage is adjusted individually and their control is decoupled.
- This method can be extended to higher-level FC converters and can be easily implemented with a typical DSP controller.

REFERENCES

[1] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[5] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *Eur. Power Electron. Drives J.*, vol. 2, no. 1, pp. 45–50, 1992.

[6] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static VAr generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.

[7] X. Yuan, H. Stemmler, and I. Barbi, "Investigation on the clamping voltage self-balancing of the three-level capacitor clamping inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1999, vol. 2, pp. 1059–1064.

[8] S. G. Lee, D. W. Kang, Y. H. Lee, and D. S. Hyun, "The carrier-based PWM method for voltage balance of flying capacitor multilevel inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, Vancouver, BC, Canada, Jun. 17–21, 2001, vol. 1, pp. 126–131.

[9] B. M. Song, J. Kim, J. S. Lai, K. C. Seong, H. J. Kim, and S. S. Park, "A multilevel soft-switching inverter with inductor coupling," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 628–636, Mar./Apr. 2001.

[10] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 809–815, Aug. 2002.

[11] D. W. Kang, W. K. Lee, and D. S. Hyun, "Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter," *Proc. Inst. Elect. Eng.*, vol. 151, no. 2, pp. 239–248, 2004.

[12] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: active control and observation of flying-capacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, Oct. 2002.

[13] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, Jun. 1997.

[14] J. P. Lavieville, O. Bethoux, P. Carrere, and T. A. Meynard, "Electronic Circuit for Converting Electrical Energy," U.S. Patent 57 268 70, 1998.

[15] J. P. Lavieville and J. Gonzalez, "Multilevel Power Converter With Self-Correction Capacitor Charge Timing Adjustment," U.S. Patent 58 285 61, 1998.

[16] L. Xu and V. G. Agelidis, "Active capacitor voltage control of flying capacitor multilevel converters," *Proc. Inst. Elect. Eng.*, vol. 151, no. 3, pp. 313–320, May 2004.

[17] B. M. Song, J. S. Lai, C. Y. Jeong, and D. W. Yoo, "A soft-switching high-voltage active power filter with flying capacitors for urban Maglev system applications," in *Proc. IEEE/IAS Annu. Meeting*, Chicago, IL, 2001, vol. 3, pp. 1461–1468.

[18] J. Holtz, W. Lotzkat, and K. H. Werner, "A high-power multitransistor-inverter uninterruptible power supply system," *IEEE Trans. Power Electron.*, vol. PE-3, no. 3, pp. 278–285, May 1988.

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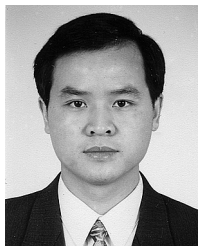

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